Code No: D5707 **R09**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH II - SEMESTER EXAMINATIONS, APRIL/MAY 2012
VLSI SIGNAL PROCESSING
(VLSI SYSTEM DESIGN)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks
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1. Give the applications of Adaptive Filters and explain the following
   a) LMS Adaptive Filter
   b) Stochastic -Gradient Adaptive Lattice Filter.

2. Explain a 3 tap FIR filter using:
   a) Block diagrams.
   b) Signal flow graphs.
   c) Data flow graphs.

3. Explain the Parallel FIR System design with example.

4. Explain register minimization using folded architectures for the following:
   a) Bi Quad filter.
   b) IIR filters.

5. Explain the design of Systolic Arrays for Matrix-Matrix Multiplication.

6. Construct a 2*3 convolution algorithm using modified wino-grad algorithm with $m(p)=p(p-1)(p+1)$.

7. Explain
   a) Path Balancing
   b) Transistor and Gate Sizing
   c) Clocking
   d) Voltage Scaling and Multiple Supply Voltages

8. Explain processors for multimedia signal processing.

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